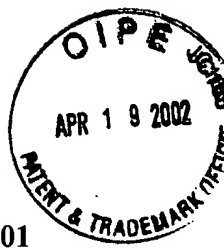


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21

Appl. No. : 09/989,563
Filed : November 19, 2001



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transistor 367 at a node 361. A second terminal of the resistor 347 is connected to ground.

REMARKS

Claims 1-25 are pending in the present application. In the January 15, 2002 Office Action, the Examiner rejects Claims 1-25 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 17-23, 26, 33, 34, and 36-39 of Application No. 09/387,263. The Examiner rejects Claim 22-24 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art. The Examiner also rejects Claims 22-24 under 35 U.S.C. § 112, second paragraph, as being indefinite. The Examiner rejects Claims 1-25 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,483,486 to Javanifard, et al., in view of U.S. Patent No. 5,473,277 to Furumochi.

Claims 1-25 remain as previously submitted. As set forth in detail below, Applicants respectfully traverse the Examiner's rejections of the claims. Applicants respectfully request allowance of Claims 1-25.

Response to Rejection of Claims 1-25 Under Obviousness-Type Double Patenting

The Examiner rejects Claims 1-25 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 17-23, 26, 33, 34, and 36-39 of Application No. 09/387,263. In addition, the Examiner states: "Although the conflicting claims are not identical, they are not patentably distinct from each other because they both recite the same scope." Applicants respectfully disagree with the Examiner's statement that both sets of claims recite the same scope. However, in order to expedite prosecution of this application, Applicants will submit a terminal disclaimer to overcome the judicially created obviousness-type double patenting rejection when the claims are found to be otherwise allowable.

Response to Rejection of Claims 22-24 Under 35 U.S.C. § 112, First Paragraph

The Examiner rejects Claims 22-24 under 35 U.S.C. § 112, first paragraph, because the specification fails to teach the step of "irreversibly by passing at least one of the plurality of

Appl. No. : 09/989,563
Filed : November 19, 2001

voltage control elements.” Applicants respectfully submit that the specification, for example, page 13, paragraphs 41 and 42, teaches the step of “irreversibly by passing at least one of the plurality of voltage control elements.” For example, paragraph 41 of the specification states that either or both of the fuses 415 and 420 may be blown. If both fuses 415 and 420 are blown, the voltage control elements, i.e., diodes 311 and 313, are effectively removed from the circuit. If only fuse 420 is blown, only the diode 313 would be removed from the circuit. See Figure 4A and page 13, paragraph 41. Thus, once a fuse is blown, the voltage control element corresponding to the blown fuse is irreversibly bypassed. Therefore, Applicants respectfully submit that the specification enables one skilled in the art to make and/or use the invention as recited in Claims 22-24.

In view of the foregoing, Applicants respectfully request the Examiner to withdraw the rejection of Claims 22-24 under 35 U.S.C. § 112, first paragraph.

Response to Rejection of Claims 22-24 Under 35 U.S.C. § 112, Second Paragraph

The Examiner rejects Claims 22-24 under 35 U.S.C. § 112, second paragraph, as being indefinite. In particular, the Examiner states:

Claim 22 is misdescriptive and renders the claim indefinite. It is misdescriptive for reciting “irreversibly” by passing at least one of the plurality of voltage control elements by transistors 425 and 430. Figure 4A shows “reversibly” by passing at least one of the plurality of voltage control elements by transistors 425 and 430.

The Examiner’s statement incorrectly describes the operations of the circuit shown in Figure 4A. Transistors 425 and 430 do not control whether the voltage control elements are irreversibly bypassed. Rather, it is the fuse 420 that controls whether the voltage control element 313 is irreversibly bypassed. As stated above, once a fuse is blown, the voltage control element corresponding to the blown fuse is irreversibly bypassed. Therefore, Applicants respectfully submit that Claims 22-24 are not indefinite.

In view of the foregoing, Applicants respectfully request the Examiner to withdraw the rejection of Claims 22-24 under 35 U.S.C. § 112, second paragraph.

Appl. No. : 09/989,563
Filed : November 19, 2001

Response to Rejection of Claims 1-25 Under 35 U.S.C. § 103(a)

The Examiner rejects Claims 1-25 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,483,486 to Javanifard, et al., in view of U.S. Patent No. 5,473,277 to Furumochi. The Examiner asserts that Javanifard discloses a circuit comprising a reference circuit 316, a voltage regulator 318 electrically coupled to the reference circuit which generates a first control signal (REG), and a charge pump 320 which receives the control signal from the voltage regulator 318, the charge pump generating the test supply voltage (Vout). Therefore, the Examiner asserts that Javanifard shows all the elements of Claim 1 except for the reference circuit having a plurality of voltage regulation devices and at least one bypass device connected to at least one of the plurality of voltage regulation devices. Furthermore, the Examiner states that Figure 5 of Furumochi shows "a reference circuit having a plurality of voltage regulation devices (T1-T4) and at least one bypass device (SW0) connected to at least one of the plurality of voltage regulation devices." The Examiner also states that "it would have been obvious to one having ordinary skill in the art to use Furumochi's figure for Javanifard et al.'s reference circuit for the purpose of generating a variable reference voltage, therefore controlling the output level of the charge pump." Moreover, the Examiner states that with the combination, it is inherent that the at least one bypass device is activated following the certification of the semiconductor device to bypass the at least one of the plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit, the voltage regulator generating a second control signal responsive to the lowered clamping threshold of the clamp circuit to cause the charge pump to generate the operational supply voltage. For the reasons set forth below, Applicants respectfully disagree.

Claims 1, 4, 15 and 25

Claims 1, 4, 15 and 25 recite a voltage control circuit comprising, among other elements, a clamp circuit having a plurality of voltage regulation devices, the voltage regulation devices controlling a clamping threshold of the clamp circuit. The voltage control circuit allows the output voltage of the charge pump to vary as the input voltage varies; however, the clamp circuit

Appl. No. : 09/989,563
Filed : November 19, 2001

limits the output voltage of the charge pump to a clamping threshold so that the safe operating voltage of the charge pump is not exceeded. That is, the magnitude of the clamped voltage is allowed to vary below the clamping threshold, but is clamped so that the magnitude of the clamped voltage cannot exceed the clamping threshold.

Neither Javanifard nor Furumochi teaches or suggests a voltage control circuit having a clamp circuit, which limits the output voltage of the charge pump to a clamping threshold. The voltage reference circuit 316 (Figure 14) of Javanifard and the constant voltage generator circuit (Figure 5) of Furumochi produce constant voltages. In column 19 at lines 22-24, Javanifard describes the voltage reference circuit 316 as "us[ing] the input voltage V_{in} to generate a reference voltage V_{ref} that is supplied to the positive terminal of VCO 318." The voltage reference circuit of Javanifard does not limit the supply voltage as would a clamp circuit. Instead, the voltage reference circuit provides a reference voltage in response to the input voltage. In column 7 at lines 15-17, Furumochi states that Figure 5 shows a constant voltage generator circuit for supplying a constant voltage to a load circuit. Furumochi does not teach or suggest that the input voltage V_{CC} ever decreases in magnitude. A reference voltage that is maintained at a constant level is entirely different from a clamped voltage, which can vary below the clamping level, but which cannot increase beyond the clamping level. Hence, there is no teaching or suggestion whatsoever in Javanifard that the reference circuit 316 is a clamp circuit or in Furumochi that the constant voltage generator circuit is a clamp circuit.

Furthermore, the Examiner suggests combining Furumochi's transistors T1-T4 and switching element SW0 with Javanifard's circuit; however, this combination would not include all the elements recited in Claims 1, 4, 15 and 25 and would not make Claims 1, 4, 15 and 25 obvious. In addition to the reasons discussed above, this combination does not teach or suggest a bypass device to bypass the at least one of the plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit. Figure 5 of Furumochi shows two transistors T4 and TN4, both of which are n-type field effect transistors having the same voltage drop from the source to the drain. (See col. 7, lines 23-25 and 45-46.) Therefore, transistor TN4 does not lower the clamping threshold of the clamp circuit. Furthermore,

Appl. No. : 09/989,563
Filed : November 19, 2001

Furumochi does not teach or suggest that the switching element SW0(TN4) lowers the clamping threshold of the circuit. Hence, the switching element SW0(TN4) is not a bypass device that lowers the clamping threshold of the clamp circuit as recited in Claims 1, 4, 15 and 25.

Because Claims 1, 4, 15 and 25 include elements not found in Javanifard or Furumochi, Applicants respectfully request the Examiner to withdraw the rejection of Claims 1, 4, 15 and 25 under 35 U.S.C. § 103(a) and to pass Claims 1, 4, 15 and 25 to allowance.

Claim 10

Claim 10 recites a voltage control circuit comprising, among other elements, means for controlling an output of a claim circuit. The means for controlling allows the output voltage of the charge pump to vary as the input voltage varies; however, the means for controlling prevents the output voltage from exceeding the safe operating voltage of the charge pump. That is, the means for controlling allows the output voltage to vary but does not allow the output voltage to exceed the safe operating voltage of the charge pump. The voltage reference circuit 316 (Figure 14) of Javanifard and the constant voltage generator circuit (Figure 5) of Furumochi both produce a constant voltage. Therefore, Javanifard and Furumochi, either individually or in any combination, do not teach or suggest a voltage control circuit comprising means for controlling an output of a clamp circuit. In fact, none of the references disclose a voltage control circuit comprising means for controlling an output of a clamp circuit. Applicants respectfully submit that Claim 10 is patentably distinguished over the cited references. Applicants respectfully request the Examiner to withdraw the rejection of Claim 10 and to pass Claim 10 to allowance.

Claim 17

Claim 17 recites a method of providing a first supply voltage on a semiconductor device during a first period and a second supply voltage during a second period, the method including the steps of generating the first supply voltage from the first voltage control signal, reversibly bypassing at least one of the plurality of voltage control elements, establishing a second voltage control signal from the plurality of voltage control elements which are not reversibly bypassed, and generating the second supply voltage from the second voltage control signal. In Claim 17,

Appl. No. : **09/989,563**
Filed : **November 19, 2001**

the first supply voltage is generated from the first voltage control signal. Thereafter, the at least one of the plurality of voltage control elements is reversibly bypassed and a second voltage control signal is established from the plurality of voltage control elements which are not reversibly bypassed. A second supply voltage is generated from the second voltage control signal.

Although the Examiner contends that the cited references show all the elements of Claim 17, Applicants respectfully submit that the references having bypass circuits do not show the steps of generating the first supply voltage from the first voltage control signal and reversibly bypassing at least one of the plurality of voltage control elements. In a further step, a second voltage control signal is established from the plurality of voltage control elements which are not reversibly bypassed. Then, in a still further step, a second supply voltage is generated from the second voltage control signal. None of the references show generating a first supply voltage, reversibly bypassing at least one of the plurality of voltage control elements, establishing a second voltage control signal from the plurality of voltage control elements which are not reversibly bypassed, and generating the second supply voltage from the second voltage control signal. Applicants respectfully submit that Claim 17 is patentably distinguished over the cited references. Applicants respectfully request the Examiner to withdraw the rejection of Claim 17 and to pass Claim 17 to allowance.

Claims 2-3, 5-9, 11-14, 16 and 18-24

Claims 2-3 and 6-9 depend from Claim 1 and further define the invention defined in Claim 1. Claim 5 depends from Claim 4 and further defines the invention defined in Claim 4. Claims 11-14 depend from Claim 10 and further define the invention defined in Claim 10. Claim 16 depends from Claim 15 and further defines the invention defined in Claim 15. Claims 18-24 depend from Claim 17 and further define the invention defined in Claim 17. In view of the foregoing remarks regarding the patentability of Claims 1, 4, 10, 15, 17 and 25, Applicants respectfully submit that dependent Claims 2-3, 5-9, 11-14, 16 and 18-24 are also patentable. Applicants respectfully request the Examiner to withdraw the rejection of Claims 2-3, 5-9, 11-14, 16 and 18-24 and to pass Claims 2-3, 5-9, 11-14, 16 and 18-24 to allowance.

Appl. No. : 09/989,563
Filed : November 19, 2001



Summary

In view of the foregoing amendments and remarks, Applicants respectfully submit that Claims 1-25 are in condition for allowance, and Applicants respectfully request allowance of Claims 1-25.

If there is any further impediment to the prompt allowance of this application, the Examiner is respectfully requested to call the undersigned attorney of record at 949-721-2849 or at the telephone number listed below.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: APRIL 15, 2002

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APR 22 2002
TECHNOLOGY CENTER 2800

Appl. No. : 09/989,563
Filed : November 19, 2001

VERSION OF SPECIFICATION WITH MARKINGS TO SHOW MODIFICATIONS

[0026] The control circuit 230 comprises a resistor 347, transistors 341, 343, 345, 353, 355, 357, 359, 363, 365, 367, 369, 371, 373, 375, and 377, and inverters 379, 383, 385, and 387. The gates of the transistors 341, 343, 345, 355, 357, and 359 are connected together and are connected to the node 335 from the voltage regulator 220. A drain of the transistor 341 is connected to the regulated voltage V_{CCR} . A source of the transistor 341 is connected to a drain of the transistor 343. A source of the transistor 343 is connected to a drain of the transistor 345. A source of the transistor [343] 345 is connected to a first terminal of the resistor 347, to a source of the transistor 359, to a gate of the transistor 365, and to a gate of the transistor 367 at a node 361. A second terminal of the resistor 347 is connected to ground.